What is Claimed is:

1. A method of providing a single scan chain of a chip, the method comprising:

selecting a TOP chain of the chip, the chip being divided into a plurality of embedded logic test (ELT) blocks;

bypassing periphery flops of the plurality of ELT blocks;

selecting a single scan chain of all ELT blocks of the chip; and

inserting the single scan chain of all ELT blocks of the chip into the TOP chain of the chip.

2. The method of claim 1 wherein the chip division is performed in a substantially hierarchical manner.

3. The method of claim 1 wherein the selecting a TOP chain is accomplished by putting the TOP chain of the chip into an internal mode.

4. The method of claim 3 wherein the TOP chain is put into internal mode by issuing an instruction to a test access port (TAP).

5. The method of claim 1 wherein a chip single chain mode is indicated by setting a user index register (IR) bit to a predefined value.

6. The method of claim 5 wherein the IR bit activates a signal sent to a test access port (TAP).

7. The method of claim 1 wherein the bypassing is accomplished by use of a plurality of multiplexers.

8. The method of claim 1 wherein the selecting a single scan chain of all ELT blocks is accomplished by putting all ELT block of the chip into an internal mode.

9. The method of claim 8 wherein the putting into internal mode is accomplished by issuing an instruction to a test access port (TAP).

10. The method of claim 1 further including selecting a plurality of blocks within a test access port (TAP) block.

11. The method of claim 10 wherein the plurality of blocks within TAP are selected from a group comprising a device identity chain block and a bypass block.

12. The method of claim 1 further including re-circulating data back to a scan chain for restoring the pre-scandump state of the chip after a scandump.

13. The method of claim 12 wherein the re-circulating is performed by utilizing a multiplexer.

14. An apparatus comprising:

a first selector to select a TOP chain of a chip, the chip being divided into a plurality of embedded logic test (ELT) blocks;

a bypassing mechanism to bypass periphery flops of the plurality of ELT blocks;

a second selector to select a single scan chain of all ELT blocks of the chip; and

a combiner to combine the single scan chain of all ELT blocks of the chip with the TOP chain of the chip,

wherein the apparatus provides a single scan chain of the chip.

15. The apparatus of claim 14 wherein the chip division is performed in a substantially hierarchical manner.

16. The apparatus of claim 14 wherein the first selector puts the TOP chain of the chip into an internal mode.

17. The apparatus of claim 16 wherein the TOP chain is put into internal mode by issuing an instruction to a test access port (TAP).

18. The apparatus of claim 14 wherein the bypassing mechanism includes a plurality of multiplexers.

19. The apparatus of claim 14 wherein the second selector puts all ELT block of the chip into an internal mode.

20. The apparatus of claim 19 wherein the putting into internal mode is accomplished by issuing an instruction to a test access port (TAP).

21. An apparatus for providing a single scan chain of a chip, the apparatus comprising:

first selection means to select a TOP chain of the chip, the chip being divided into a plurality of embedded logic test (ELT) blocks;

bypassing means for bypassing periphery flops of the plurality of ELT blocks;

second selection means to select a single scan chain of all ELT blocks of the chip; and

inserting means to insert the single scan chain of all ELT blocks of the chip into the TOP chain of the chip.

22. The apparatus of claim 21 further including a plurality of multiplexers.

23. An article of manufacture comprising:

a machine readable medium that provides instructions that, if executed by a machine, will cause the machine to perform operations including:

selecting a TOP chain of a chip, the chip being divided into a plurality of embedded logic test (ELT) blocks;

bypassing periphery flops of the plurality of ELT blocks;

selecting a single scan chain of all ELT blocks of the chip; and

inserting the single scan chain of all ELT blocks of the chip into the TOP chain of the chip,

wherein the operations provide a single scan chain of the chip.

24. The article of claim 23 wherein the chip division is performed in a substantially hierarchical manner.

25. The article of claim 23 wherein the selecting a TOP chain is accomplished by putting the TOP chain of the chip into an internal mode.

26. The article of claim 25 wherein the TOP chain is put into internal mode by issuing an instruction to a test access port (TAP) unit.

27. The article of claim 23 wherein the bypassing is accomplished by use of a plurality of multiplexer procedures.

28. The article of claim 23 wherein the selecting a single scan chain of all ELT blocks is accomplished by putting all ELT block of the chip into an internal mode.

29. The article of claim 28 wherein the putting into internal mode is accomplished by issuing an instruction to a test access port (TAP) unit.

30. The article of claim 29 wherein the operations further include selecting a plurality of blocks within a test access port (TAP) unit.

31. The article of claim 30 wherein the plurality of blocks within TAP are selected from a group comprising a device identity chain block and a bypass block.

32. The article of claim 23 wherein the operations further include re-circulating data back to a scan chain for restoring the pre-scandump state of the chip after a scandump.

33. The article of claim 32 wherein the re-circulating is performed by utilizing a multiplexer procedure.